spends exactly to calculations for the case of 20 dB suppression of \(10^3\) BER and a 44 dB CNR (at \(10^3\) BER) which is achieved by considering the influence of the linewidth of lasers.

![Fig. 3 Measured BERs of IRR and with image band signal 560 Mbps DSSS](image)

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**Fig. 4** shows crosstalk penalties (defined by the power penalty at \(10^3\) BER) as a function of the channel allocation.

- The power penalty without the IRR is shown by \(\circ\), and the power penalty with the IRR is shown by \(\bullet\).
- When the image band signal overlaps the real band signal in the IF domain, the signal cannot be received without the IRR, whereas the power penalty is less than 1-4 dB with the IRR. Crosstalk penalties agreed well with the calculations (solid lines), taking into account the suppression of the IRR. When penalties of less than 1-4 dB are permitted, the channel spacing must be set to 11 times wider than a bit rate without the IRR, whereas it can be set to about 3 times wider with the IRR.

The wrapper does not show the IRR, the less crosstalk penalties between signal lightwaves. The two outputs of the \(90^\circ\) optical hybrid circuit must have a good balance in gain and phase. The calculated crosstalk penalties due to the \(90^\circ\) optical hybrid circuit misalignment are shown in Fig. 5. The combination of gain and phase difference which intercept this curve, or within the enclosed area, gives performance degradations of 1 and 0-5 dB.

![Fig. 5 Calculated crosstalk penalties due to \(90^\circ\) optical hybrid circuit misalignment](image)

**Conclusion:** We demonstrated an optical-frequency IRR which provides more than 18 dB suppression over the 15-17 GHz IF region. The measured crosstalk penalties as a function of the channel allocation were less than 1-4 dB in a 2-channel 560 Mbps DSSS DSIPK heterodyne optical communication system using the IRR. These results promise the possibility of the application of this scheme to high-density OFDM.

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**STOCHASTIC RELAXATION ALGORITHM FOR IMPROVED VECTOR QUANTISER DESIGN**

**Indexing terms:** Image processing, Algorithms, Speech processing, Quantisers

An easily implementable stochastic relaxation algorithm for vector quantisation design is given. It generalises the usual Lloyd iteration in codebook design by perturbing the computed centroids with independent multidimensional noise, whose variance diminishes as the algorithm progresses. A significant improvement is often achieved.

**Introduction:** The design of vector quantisers plays an important role in developing high-quality voice and image communication systems. The traditional approach, called the LBG algorithm or generalized Lloyd algorithm (GLA), iteratively updates the encoder and decoder of a quantiser according to the well-known nearest neighbour (NN) and centroid conditions. Each iteration results in a strict decrease in average

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The variance of the noise (i.e. the temperature) decreases (cools) as the algorithm progresses. The critical difference between this algorithm and SA is that the codevector perturbations are accepted unconditionally, whereas in SA their acceptance depends probabilistically on the values of $\Delta E$ and $T$. This is significant because it completely eliminates the need to compute the change in energy $\Delta E$ at each iteration.

Codebook design algorithm:

(a) Codevector initialisation: $v_1^s, \ldots, v_K^s$.

(b) Nearest neighbour repartition ($1 \leq k \leq N$):

\[ j = \arg \min_{k \neq 1} (x_n - y_k)^2 \leq 1 \leq N \]

Let $k \in R_i$

\[ D_k = D_{1k} + (x_n - y_k)^2 \]

(c) Stoppage criterion:

\[ \text{stop} \iff D_{1k} - D_k c < \text{stop} \]

\[ m = m + 1 \]

(d) Centroid computation ($1 \leq k \leq N$):

\[ x_{n+1}^k = \frac{1}{|R_k|} \sum_{x \in R_k} x \]

(e) Codevector jiggling ($1 \leq k \leq N$):

\[ (y_k - x_{n+1}^k) + \beta \tilde{y} \]

Goto (b)

Temperature schedule: There are many different temperature schedules that can be used to cool the system. Generally in SA algorithms the slower the cooling, the closer one gets to the global optimum. If the number of iterations is constrained then it is generally better to cool the system relatively fast at the beginning and then gradually approach freezing with slow temperature decreases.

Experimentally we have found that a reasonable initial temperature is on the order of the input variance $\sigma^2$. Three classes of cooling functions were investigated, one of which explicitly depends on a bound $D$ on the total number of iterations allowed, various choices for the parameters $p$ and $c$ can be utilised. The dependence of the algorithm's performance on the temperature schedule was significant, though the best schedule often varied somewhat depending on which source was used. The various cooling schedules are given below:

(a) $T_n = \sigma^2 \left(1 - \frac{n}{D} \right)$

(b) $T_n = \sigma^2 \left(1 - \frac{n}{p} \right)$

(c) $T_n = \sigma^2 \left(1 - \frac{n}{m} \right)$

In (a) with $p$ taking the values 1, 2, or 3 were tested. In (b) $m$ was fixed to equal to 2, 1 or 1. In (a) the best results occurred with $p = 3$ and in (b) with $p = 3$. In (c) we chose $m = 995$, though other values also yield good results. The best schedule overall, of those we tested, appeared to be in (a) with $p = 3$. Fig. 1 shows a comparison of the performance of the above algorithm and the GLA for a speech signal sampled at 8kHz and scalar-quantised with a codebook of size 32. The two functions plotted are the signal-to-noise ratios of the quantisers as a function of the algorithm's iteration number. In this example, a 0.8 dB gain was achieved.
INJECTION TRANSISTOR LOGIC (ITL): NEW BIPOLAR LOW-POWER INVERTER

Indexing terms: Semiconductor devices and materials, Bipolar devices, Logic devices, Inverter.

We investigate the characteristics of a new injection transistor logic (ITL), fabricated by vapour-phase epitaxy and ion implantation. The optimum current gain of the BJT-inverter is about 150. The propagation delay of was determined by the rise and transmission frequency method. At a power of 50µW per gate for the inverter, it is about 500ns and 850ns for 60µW. In the high-speed ITL inverter it is about 25µs for 150µW.

Integrated injection logic (IITL) was introduced in 1972. It is a bipolar logic device using vertical inverse-operated n-p-n transistors with multiplate collectors as inductors and lateral p-p-n transistors as current sources. However, ITL has comparatively low-speed performance and other characteristics. In this letter we show the results of experimental

investigations of injection transistor logic (ITL). It is a new, similar, saturating bipolar structure which provides the speed, power and density suitable for VLSI. This merged complementarity structure is realised by a vertical npn transistor operated in a downslope mode and a vertical p-p-n supply device in downward mode. The ITL devices can be classified as the separate subclass of logic devices with an injection source. The advantages of these devices include high-speed performance, high-current gain and low-power consumption.

The devices were fabricated on a 100Om, p-type, 100-orientation Si-substrate by implanting Sh in the substrate through windows etched in silicon dioxide. The carrier concentration and thickness of the buffer layer were , and respectively, and the Si0.35 layer, transport vapour-phase epitaxy. Further, the isolation regions were formed by selective oxidation of silicon . Then, through the SI0.35 layer, 0.3µm and the emulsion layer, 0.5 regions ( ) were realised by implanting boron. An active n-region of the pnp transistor ( ) was formed by implanting arsenic . An epitaxial layer through windows etched in Si0.35. The injector p+ regions were realised by implanting boron through the SI0.35 layer and the emulsion layer. After pulse laser annealing and cleaning processes, PLS-TW-10 Al ohmic contacts were evaporated and annealed for 9min at 700K in an N2 atmosphere. The thicknesses of the base regions of npn and pnp transistors were 0.2µm and 0.3µm, respectively.

Fig. 1 Schematic structures and circuits of Si-injection-transistor logic:

- Basic structures ITL
- High-speed structures ITL

Fig. 1 shows the structures and circuits of the ITL inverter in the basic and high-speed construction. The devices were fabricated into planar structures with emitter length and width 9µm and 4µm, respectively. Horizontal ITL-inverter sizes were as follows: length and width were 32µm and 4µm, respectively; emitter-base spacing was 6µm; emitter-injector spacing was 6µm. For limitation of the high-speed ITL structure (Fig. 1b), we used the voltage source for .

Fig. 2 shows the current gain complementary transistors of the ITL-inverter against the current density at 300K. The maximum current gain of the switching npn transistor was about 150. The current gain of the npn current source was 55. The high current gain of an npn transistor provides a fan-out of about 90.

The propagation delay of the ITL-inverter against the power consumption of the oscillator p-n gate at 300K is