CHAPTER

11

FIELD-EFFECT TRANSISTORS: OPERATION, CIRCUIT MODELS, AND APPLICATIONS

Chapter 11 introduces the family of field-effect transistors, or FETs. The concept that forms the basis of the operation of the field-effect transistor is that an external electric field may be used to vary the conductivity of a *channel*, causing the FET to behave either as a voltage-controlled resistor or as a voltage-controlled current source.

FETs are the dominant transistor family in today's integrated electronics, and although these transistors come in several different configurations, it is possible to understand the operation of the different devices by focusing principally on one type.

In this chapter we focus on the basic operation of the enhancement-mode, metal-oxide-semiconductor FET, leading to the technologies that are commonly known as NMOS, PMOS, and CMOS. The chapter reviews the operation of these devices as large-signal amplifiers and as switches.

Learning Objectives

1. Understand the classification of field-effect transistors. *Section 11.1.*
2. Learn the basic operation of enhancement-mode MOSFETs by understanding their i–v curves and defining equations. *Section 11.2.*
3. Learn how enhancement-mode MOSFET circuits are biased. *Section 11.3.*
4. Understand the concept and operation of FET large-signal amplifiers. *Section 11.4.*
5. Understand the concept and operation of FET switches. *Section 11.5.*
6. Analyze FET switches and digital gates. *Section 11.5.*

LO1

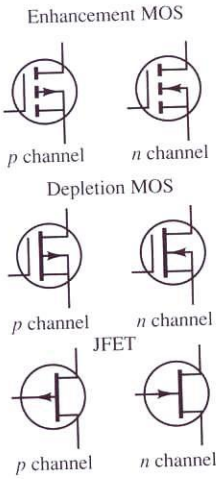


Figure 11.1 Classification of field-effect transistors

11.1 CLASSIFICATION OF FIELD-EFFECT TRANSISTORS

Figure 11.1 depicts the classification of field-effect transistors, as well as the more commonly used symbols for these devices. These devices can be grouped into three major categories. The first two categories are both types of **metal-oxide semiconductor field-effect transistors,** or **MOSFETs: enhancement-mode MOSFETs** and **depletion-mode MOSFETs.** The third category consists of **junction field-effect transistors,** or **JFETs.** In addition, each of these devices can be fabricated either as an ***n*-channel** device or as a ***p*-channel** device, where the n or p designation indicates the nature of the doping in the semiconductor channel. All these transistors behave in a very similar fashion, and we shall predominantly discuss enhancement MOSFETs in this chapter, although a brief discussion of depletion devices and JFETs is also included.

11.2 OVERVIEW OF ENHANCEMENT-MODE MOSFETS

Figure 11.2 depicts the circuit symbol and the approximate construction of a typical n-channel enhancement-mode MOSFET. The device has three terminals: the **gate** (analogous to the base in a BJT), the **drain** (analogous to the collector), and the **source** (analogous to the emitter). The **bulk** or **substrate** of the device is shown to be electrically connected to the source, and therefore it does not appear in the electric circuit diagram as a separate terminal. The gate consists of a metal film layer, separated from the p-type bulk by a thin oxide layer (hence the terminology *metal-oxide semiconductor*). The drain and source are both constructed of n^+ material.

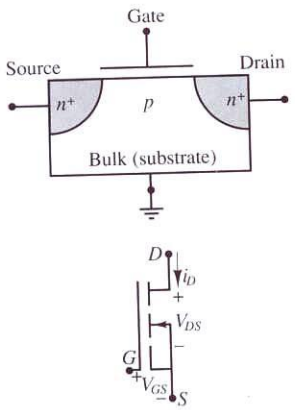


Figure 11.2 The n-channel enhancement MOSFET construction and circuit symbol

Imagine now that the drain is connected to a positive voltage supply V_{DD}, and the source is connected to ground. Since the p-type bulk is connected to the source, and hence to ground, the drain-bulk n^+p junction is strongly reverse-biased. The junction voltage for the pn^+ junction formed by the bulk and the source is zero, since both are connected to ground. Thus, the path between drain and source consists of two reverse-biased pn junctions, and no current can flow. This situation is depicted in Figure 11.3(a): in the absence of a gate voltage, the n-channel enhancement-mode MOSFET acts as an open circuit. Thus, enhancement-mode devices are *normally off.*

Suppose now that a positive voltage is applied to the gate; this voltage will create an electric field in the direction shown in Figure 11.3(b). The effect of the electric

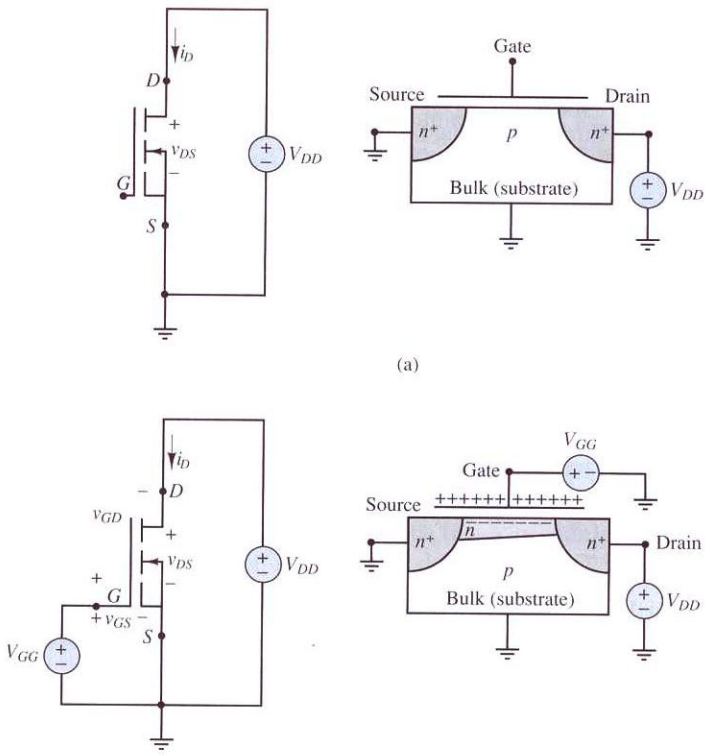


Figure 11.3 Channel formation in NMOS transistor: (a) With no external gate voltage, the source-substrate and substrate-drain junctions are both reverse-biased, and no conduction occurs; (b) when a gate voltage is applied, charge-carrying electrons are drawn between the source and drain regions to form a conducting channel.

field is to repel positive charge carriers away from the surface of the p-type bulk, and to form a narrow **channel** near the surface of the bulk in which negative charge carriers dominate and are available for conduction. For a fixed drain bias, the greater the strength of the externally applied electric field (i.e., the higher the gate voltage), the higher the concentration of carriers in the channel, and the higher its conductivity. This behavior explains the terminology *enhancement mode*, because the application of an external electric field *enhances* the conduction in the channel by creating n-type charge carriers. It should also be clear why these devices are called *field-effect*, since it is an external electric field that determines the conduction properties of the transistor.

It is also possible to create *depletion-mode* devices in which an externally applied field depletes the channel of charge carriers by reducing the effective channel width. Depletion-mode MOSFETs are normally on, and they can be turned off by application of an external electric field.

To complete this brief summary of the operation of MOS transistors, we note that, in analogy with *pnp* bipolar transistors, it is also possible to construct p-channel MOSFETS. In these transistors, conduction occurs in a channel formed in n-type bulk material via positive charge carriers.

We first define a few key parameters that generally apply to enhancement-mode and depletion-mode and to n-channel as well as p-channel devices.

Threshold Voltage, V_T

When the gate-to-substrate voltage is greater than the threshold voltage, a conducting channel is formed through the creation of a layer of free electrons. In enhancement-mode devices, the threshold voltage is positive. If at any location between the source and drain regions of the transistor the gate-to-substrate voltage is greater than the threshold voltage, then the channel is said to be *on* at that point. Otherwise the channel is *off*, and no current can flow.

In depletion-mode devices, a conducting n-type channel is built into the device by design, and a negative gate-to-substrate voltage is used to turn the channel off (depleting the n-type channel of electrons—hence the name *depletion mode*). We shall not discuss depletion-mode devices any further in this book.

Conductance Parameter K

The ability of the channel to conduct is dependent on different mechanisms, which are captured in a conductance parameter K, defined as

$$K = \frac{W}{L}\frac{\mu C_{ox}}{2} \tag{11.1}$$

In equation 11.1, W represents the width of the channel, L represents the length, μ is the mobility of the charge carrier (electrons in n-channel devices, holes in p-channel devices), and C_{ox} is the capacitance of the oxide layer.

Early Voltage V_A

This parameter describes the dependence on v_{DS} of the MOSFET drain current in the saturation region. It is common to assume that V_A approaches infinity, indicating that the drain current is independent of v_{DS}. The role of this parameter will become more obvious in the next section.

Operation of the *n*-Channel Enhancement-Mode MOSFET

We first focus on n-channel enhancement mode transistors, which are generally referred to as NMOS devices. The operation of these devices is most effectively explained by making reference to the four-quadrant plot of Figure 11.4. In this figure, the behavior of the NMOS device is tied to whether the channel is on or off at the source or drain end of the transistor. Recall that whenever the gate-to-substrate voltage is higher than the threshold voltage, the channel is on.

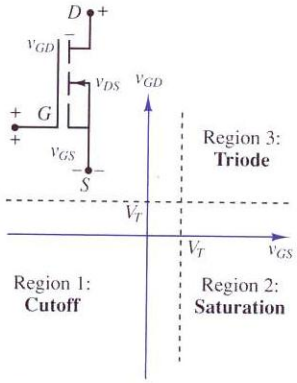


Figure 11.4 Regions of operation of NMOS transistor

Cutoff Region

When both $v_{GS} < V_T$ and $v_{GD} < V_T$, the channel is off at both the source and the drain. Thus, there is no conduction region between drain and source, and no current can be conducted. We call this the **cutoff region,** indicated in Figure 11.4 by region 1. In this region,

$$i_D = 0 \qquad \text{Cutoff region} \tag{11.2}$$

Saturation Region

When $v_{GS} > V_T$, and $v_{GD} < V_T$, the channel is on at the source end and off at the drain. In this mode, the drain current is (very nearly) independent of the

drain-to-source voltage v_{DS} and depends on only the gate voltage. We call this the **saturation region,** indicated in Figure 11.4 by region 2. In this region, the MOSFET acts as a *voltage-controlled current source*. The equation for the drain current is given in equation 11.3. Note that in the more complete form of the equation, both the parameter V_A and the drain-to-source voltage v_{DS} appear. If, as is commonly done, we assume that V_A is very large, then we can use the approximate form, also shown below, which is independent of v_{DS}.

$$i_D = K(v_{GS} - V_T)^2\left(1 + \frac{v_{DS}}{V_A}\right) \qquad \text{Saturation region} \qquad \textbf{(11.3)}$$
$$\cong K(v_{GS} - V_T)^2$$

Triode or Ohmic Region

When $v_{GS} > V_T$ and $v_{GD} > V_T$, the channel is on at both ends of the device. In this mode, the drain current is strongly dependent on both the drain-to-source voltage v_{DS} and the gate-to-source voltage v_{GS}. We call this the **triode** or **ohmic region,** indicated in Figure 11.4 by region 2. The equation for the drain current is

$$i_D = K[2(v_{GS} - V_T)v_{DS} - v_{DS}^2] \qquad \text{Triode or ohmic region} \qquad \textbf{(11.4)}$$

If v_{DS} is much smaller than v_{GS}, then $v_{GD} = v_{GS} - v_{DS} \approx v_{GS}$. Thus, for small values of v_{DS} (see the drain characteristic curves in Figure 11.5), the channel is approximately equally on at both the drain and the source end. Thus, changes in the gate voltage will directly affect the conductivity of the channel. In this mode, the MOSFET behaves very much as a *voltage-controlled resistor* that is controlled by the gate voltage. This property finds much use in integrated circuits, in that it is easier to implement an integrated-circuit version of a resistor through a MOSFET than to actually build a passive resistor. There also exist other applications of the voltage-controlled resistor property of MOSFETs in tunable (variable-gain) amplifiers and in analog gates.

The three regions of operation can also be identified in the drain characteristic curves shown in Figure 11.5. In this figure, the circuit of Figure 11.3(b) is used to vary the gate and drain voltages with respect to the source and substrate (which are assumed to be electrically connected). You can see that for $v_{GS} < V_T$ and $v_{GD} < V_T$, the transistor is in the cutoff region (1) and no drain current flows. To better understand the difference between the saturation and triode (or ohmic) regions of operation, the boundary between these two regions is shown in Figure 11.5 by the curve $i_D = K v_{DS}^2$. You can see that in the saturation region (2), the transistor supplies nearly constant drain current, the value of which is dependent on the square of the gate-to-source voltage. Thus, in this region the MOSFET operates as a *voltage-controlled current source*, and it can be used in a variety of amplifier applications. On the other hand, in the triode region (3), the drain current is very strongly dependent on both the gate-to-source and the drain-to-source voltages (see equation 11.4). If, however, v_{DS} is much smaller than v_{GS}, then $v_{GD} = v_{GS} + v_{DS} \approx v_{GS}$, and the channel is on equally, or very nearly so, at both the source and drain ends. This corresponds to the region near the origin in the curves of Figure 11.5, in which the drain current curves are nearly straight lines. In this portion of the triode region, the MOSFET acts as a variable resistor, with resistance (i.e., the reciprocal of the slope in the $i_D - v_{DS}$ curves) controlled by the gate-to-source voltage. As mentioned earlier, this variable resistor characteristic of MOSFETs is widely exploited in integrated circuits. Finally, if the drain-to-source voltage exceeds the **breakdown voltage** V_{DSS}, the drain current will

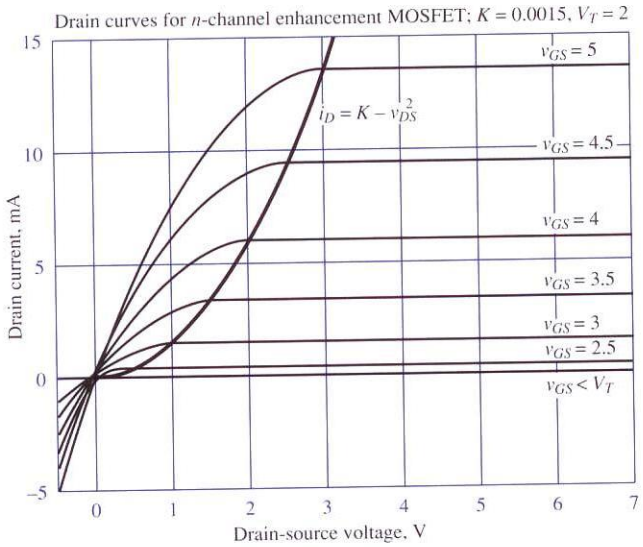


Figure 11.5 Drain characteristic curves for a typical NMOS transistor with $V_T = 2$ V and $K = 1.5$ mA/V^2

increase sharply and the result may be device failure. This **breakdown region** is not shown in Figure 11.5.

LO2

EXAMPLE 11.1 Determining the Operating State of a MOSFET

Problem

Determine the operating state of the MOSFET shown in the circuit of Figure 11.6 for the given values of V_{DD} and V_{GG} if the ammeter and voltmeter shown read the following values:

a. $V_{GG} = 1$ V; $V_{DD} = 10$ V; $v_{DS} = 10$ V; $i_D = 0$ mA; $R_D = 100\ \Omega$.

b. $V_{GG} = 4$ V; $V_{DD} = 10$ V; $v_{DS} = 2.8$ V; $i_D = 72$ mA; $R_D = 100\ \Omega$.

c. $V_{GG} = 3$ V; $V_{DD} = 10$ V; $v_{DS} = 1.5$ V; $i_D = 13.5$ mA; $R_D = 630\ \Omega$.

Solution

Known Quantities: MOSFET drain resistance; drain and gate supply voltages; MOSFET equations.

Find: MOSFET quiescent drain current, i_{DQ}, and quiescent drain-source voltage, v_{DSQ}.

Schematics, Diagrams, Circuits, and Given Data: $V_T = 2$ V; $K = 18$ mA/V^2.

Assumptions: Use the MOSFET equations 11.2–11.4 as needed.

Analysis:

a. Since the drain current is zero, the MOSFET is in the cutoff region. You should verify that both the conditions $v_{GS} < V_T$ and $v_{GD} < V_T$ are satisfied.

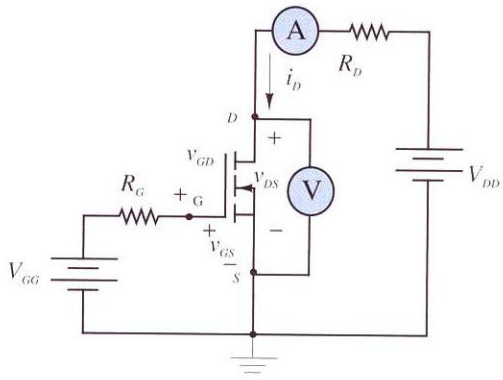


Figure 11.6 Circuit used in Example 11.1

b. In this case, $v_{GS} = V_{GG} = 4\text{ V} > V_T$. On the other hand, $v_{GD} = v_G - v_D = 4 - 2.8 = 1.2\text{ V} < V_T$. Thus, the transistor is in the saturation region. We can calculate the drain current to be: $i_D = K(v_{GS} - V_T)^2 = 18 \times (4-2)^2 = 72$ mA. Alternatively, we can also calculate the drain current as $i_D = \frac{V_{DD} - v_{DS}}{R_D} = \frac{10-2.8}{0.1\,\text{k}\Omega} = 72$ mA.

c. In the third case, $v_{GS} = V_{GG} = v_G\ 3\text{ V} > V_T$. The drain voltage is measured to be $v_{DS} = v_D = 1.5$ V, and therefore $v_{GD} = 3 - 1.5 = 1.5\text{ V} < V_T$. In this case, the MOSFET is in the ohmic, or triode, region. We can now calculate the current to be $i_D = K[2(v_{GS} - V_T)v_{DS} - v_{DS}^2] = 18 \times [2 \times (3-2) \times 1.5 - 1.5^2] = 13.5$ mA. We can also calculate the drain current to be $i_D = \frac{V_{DD} - v_{DS}}{R_D} = \frac{(10-1.5)V}{0.630\,\text{k}\Omega} = 13.5$ mA.

CHECK YOUR UNDERSTANDING

What is the operating state of the MOSFET of Example 11.1 for the following conditions?

$V_{GG} = 10/3$ V; $V_{DD} = 10$ V; $v_{DS} = 3.6$ V; $i_D = 32$ mA; $R_D = 200\ \Omega$.

Answer: Saturation

11.3 BIASING MOSFET CIRCUITS

Now that we have analyzed the basic characteristics of MOSFETs of the *n*-channel enhancement MOSFET and can identify its operating state, we are ready to develop systematic procedures for biasing a MOSFET circuit. This section presents two bias circuits. The first, illustrated in Examples 11.2 and 11.3, uses two distinct voltage supplies. This bias circuit is easier to understand, but not very practical—as we have already seen with BJTs, it is preferable to have a single DC voltage supply. This desire is addressed by the second bias circuit, described in Examples 11.4 and 11.5.

LO2

EXAMPLE 11.2 MOSFET Q-Point Graphical Determination

Problem

Determine the Q point for the MOSFET in the circuit of Figure 11.7.

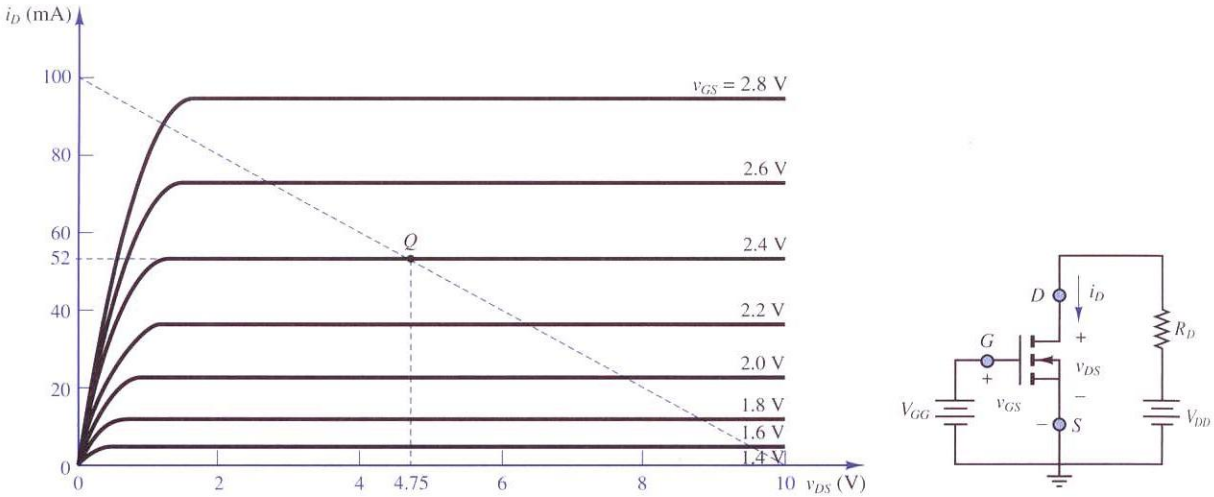


Figure 11.7 The n-channel enhancement MOSFET circuit and drain characteristic for Example 11.2

Solution

Known Quantities: MOSFET drain resistance; drain and gate supply voltages; MOSFET drain curves.

Find: MOSFET quiescent drain current i_{DQ} and quiescent drain-source voltage v_{DSQ}.

Schematics, Diagrams, Circuits, and Given Data: $V_{GG} = 2.4$ V; $V_{DD} = 10$ V; $R_D = 100\,\Omega$.

Assumptions: Use the drain curves of Figure 11.7.

Analysis: To determine the Q point, we write the drain circuit equation, applying KVL:

$$V_{DD} = R_D i_D + v_{DS}$$

$$10 = 100 i_D + v_{DS}$$

The resulting curve is plotted as a dashed line on the drain curves of Figure 11.7 by noting that the drain current axis intercept is equal to $V_{DD}/R_D = 100$ mA and that the drain-source voltage axis intercept is equal to $V_{DD} = 10$ V. The Q point is then given by the intersection of the load line with the $V_{GG} = 2.4$ V curve. Thus, $i_{DQ} = 52$ mA and $v_{DSQ} = 4.75$ V.

Comments: Note that the Q-point determination for a MOSFET is easier than for a BJT, since there is no need to consider the gate circuit, because gate current flow is essentially zero. In the case of the BJT, we also needed to consider the base circuit.

CHECK YOUR UNDERSTANDING

Determine the operating region of the MOSFET of Example 11.2 when $v_{GS} = 3.5$ V.

Answer: The MOSFET is in the ohmic region.

EXAMPLE 11.3 MOSFET Q-Point Calculation

Problem

Determine the Q point for the MOSFET in the circuit of Figure 11.7.

Solution

Known Quantities: MOSFET drain resistance; drain and gate supply voltages; MOSFET equations.

Find: MOSFET quiescent drain current i_{DQ} and quiescent drain-source voltage v_{DSQ}.

Schematics, Diagrams, Circuits, and Given Data: $V_{GG} = 2.4$ V; $V_{DD} = 10$ V; $V_T = 1.4$ V; $K = 48.5$ mA/V^2; $R_D = 100\ \Omega$.

Assumptions: Use the MOSFET equations 11.2 through 11.4 as needed.

Analysis: The gate supply V_{GG} ensures that $v_{GSQ} = V_{GG} = 2.4$ V. Thus, $v_{GSQ} > V_T$. We assume that the MOSFET is in the saturation region, and we proceed to use equation 11.3 to calculate the drain current:

$$i_{DQ} = K(v_{GS} - V_T)^2 = 48.5(2.4 - 1.4) = 48.5 \text{ mA}$$

Applying KVL to the drain loop, we can calculate the quiescent drain-to-source voltage as:

$$v_{DSQ} = V_{DD} - R_D i_{DQ} = 10 - 100 \times 48.5 \times 10^{-3} = 5.15 \text{ V}$$

Now we can verify the assumption that the MOSFET was operating in the saturation region. Recall that the conditions required for operation in region 2 (saturation) were $v_{GS} > V_T$ and $v_{GD} < V_T$. The first condition is clearly satisfied. The second can be verified by recognizing that $v_{GD} = v_{GS} + v_{SD} = v_{GS} - v_{DS} = -2.75$ V. Clearly, the condition $v_{GD} < V_T$ is also satisfied, and the MOSFET is indeed operating in the saturation region.

CHECK YOUR UNDERSTANDING

Find the lowest value of R_D for the MOSFET of Example 11.3 that will place the MOSFET in the ohmic region.

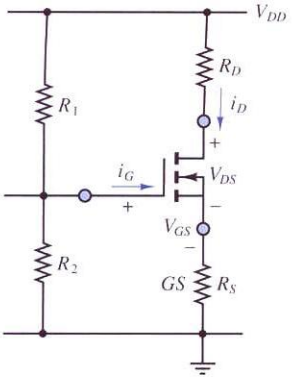
Answer: $\sim 400\ \Omega$

LO3

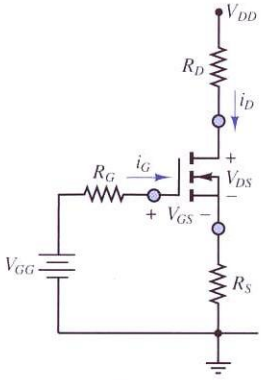
EXAMPLE 11.4 MOSFET Self-Bias Circuit

Problem

Figure 11.8(a) depicts a self-bias circuit for a MOSFET. Determine the Q point for the MOSFET by choosing R_S such that $v_{DSQ} = 8$ V.



(a)



(b)

Figure 11.8 (a) Self-bias circuit for Example 11.4; (b) equivalent circuit for (a)

Solution

Known Quantities: MOSFET drain and gate resistances; drain supply voltage; MOSFET parameters V_T and K; desired drain-to-source voltage v_{DSQ}.

Find: MOSFET quiescent gate-source voltage v_{GSQ}, quiescent drain current i_{DQ}, and quiescent drain-source voltage v_{DSQ}.

Schematics, Diagrams, Circuits, and Given Data: $V_{DD} = 30$ V; $R_D = 10$ kΩ; $R_1 = R_2 = 1.2$ MΩ; $V_T = 4$ V; $K = 0.2188$ mA/V^2; $v_{DSQ} = 8$ V.

Assumptions: Assume operation in the saturation region.

Analysis: First we reduce the circuit of Figure 11.8(a) to the circuit of Figure 11.8(b), in which the voltage divider rule has been used to compute the value of the fictitious supply V_{GG}:

$$V_{GG} = \frac{R_2}{R_1 + R_2} V_{DD} = 15 \text{ V}$$

Let all currents be expressed in milliamperes and all resistances in kilohms. Applying KVL around the equivalent gate circuit of Figure 11.8(b) yields

$$v_{GSQ} + i_{GQ} R_G + i_{DQ} R_S = V_{GG} = 15 \text{ V}$$

where $R_G = R_1 \| R_2$. Since $i_{GQ} = 0$, due to the infinite input resistance of the MOSFET, the gate equation simplifies to

$$v_{GSQ} + i_{DQ} R_S = 15 \text{ V} \qquad \textbf{(a)}$$

The drain circuit equation is

$$v_{DSQ} + i_{DQ} R_D + i_{DQ} R_S = V_{DD} = 30 \text{ V} \qquad \textbf{(b)}$$

Using equation 11.3, we get

$$i_{DQ} = K (v_{GS} - V_T)^2 \qquad \textbf{(c)}$$

We can obtain the third equation needed to solve for the three unknowns v_{GSQ}, i_{DQ}, and v_{DSQ}. From equation (a) we write

$$i_{DQ} R_S = V_{GG} - v_{GSQ} = \frac{V_{DD}}{2} - v_{GSQ}$$

and we substitute the result into equation (b):

$$V_{DD} = i_{DQ} R_D + v_{DSQ} + \frac{V_{DD}}{2} - v_{GSQ}$$

or

$$i_{DQ} = \frac{1}{R_D} \left(\frac{V_{DD}}{2} - v_{DSQ} + v_{GSQ} \right)$$

Substituting the above equation for i_{DQ} into equation (c), we finally obtain a quadratic equation that can be solved for v_{GSQ} since we know the desired value of v_{DSQ}:

$$\frac{1}{R_D}\left(\frac{V_{DD}}{2} - v_{DSQ} + v_{GSQ}\right) = K\left(v_{GSQ} - V_T\right)^2$$

$$K v_{GSQ}^2 - 2K V_T v_{GSQ} + K V_T^2 - \frac{1}{R_D}\left(\frac{V_{DD}}{2} - v_{DSQ}\right) - \frac{1}{R_D} v_{GSQ} = 0$$

$$v_{GSQ}^2 - \left(2V_T + \frac{1}{KR_D}\right) v_{GSQ} + V_T^2 - \frac{1}{KR_D}\left(\frac{V_{DD}}{2} - v_{DSQ}\right) = 0$$

$$v_{GSQ}^2 - 8.457 v_{GSQ} + 12.8 = 0$$

The two solutions for the above quadratic equation are

$$v_{GSQ} = 6.48 \text{ V} \quad \text{and} \quad v_{GSQ} = 1.97 \text{ V}$$

Only the first of these two values is acceptable for operation in the saturation region, since the second root corresponds to a value of v_{GS} lower than the threshold voltage (recall that $V_T = 4$ V). Substituting the first value into equation (c), we can compute the quiescent drain current

$$i_{DQ} = 1.35 \text{ mA}.$$

Using this value in the gate circuit equation (a), we compute the solution for the source resistance:

$$R_S = 6.32 \text{ k}\Omega$$

Comments: Why are there two solutions to the problem posed in this example? Mathematically, we know that this should be the case because the drain universal equation is a quadratic equation. As you can see, we used the physical constraints of the problem to select the appropriate solution.

CHECK YOUR UNDERSTANDING

Determine the appropriate value of R_S if we wish to move the operating point of the MOSFET of Example 11.4 to $v_{DSQ} = 12$ V. Also find the values of v_{GSQ} and i_{DQ}. Are these values unique?

Answer: The answer is not unique. For the smaller value of $v_{GS} = 2.86$ V, $R_S = 20.7$ kΩ and $i_D = 0.586$ mA. For the larger value of v_{GS}, $R_S = 11.5$ kΩ.

EXAMPLE 11.5 Analysis of MOSFET Amplifier

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Problem

Determine the gate and drain-source voltage and the drain current for the MOSFET amplifier of Figure 11.9.

Solution

Known Quantities: Drain, source, and gate resistors; *drain supply voltage; MOSFET parameters.*

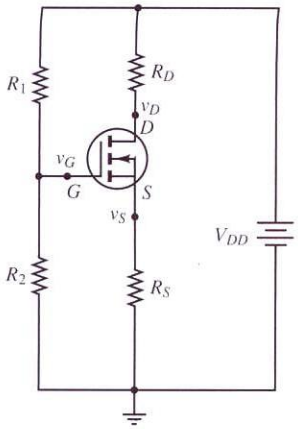

Figure 11.9

Find: v_{GS}; v_{DS}; i_D.

Schematics, Diagrams, Circuits, and Given Data: $R_1 = R_2 = 1$ MΩ; $R_D = 6$ kΩ; $R_S = 6$ kΩ; $V_{DD} = 10$ V. $V_T = 1$ V; $K = 0.5$ mA/V^2.

Assumptions: The MOSFET is operating in the saturation region. All currents are expressed in milliamperes and all resistors in kilohms.

Analysis: The gate voltage is computed by applying the voltage divider rule between resistors R_1 and R_2 (remember that no current flows into the transistor):

$$v_G = \frac{R_2}{R_1 + R_2} V_{DD} = \frac{1}{2} V_{DD} = 5 \text{ V}$$

Assuming saturation region operation, we write

$$v_{GS} = v_G - v_S = v_G - R_S i_D = 5 - 6i_D$$

The drain current can be computed from equation 11.3:

$$i_D = K\,(v_{GS} - V_T)^2 = 0.5\,(5 - 6i_D - 1)^2$$

leading to

$$36i_D^2 - 50i_D + 16 = 0$$

with solutions

$$i_D = 0.89 \text{ mA} \qquad \text{and} \qquad i_D = 0.5 \text{ mA}$$

To determine which of the two solutions should be chosen, we compute the gate-source voltage for each. For $i_D = 0.89$ mA, $v_{GS} = 5 - 6i_D = -0.34$ V. For $i_D = 0.5$ mA, $v_{GS} = 5 - 6i_D = 2$ V. Since v_{GS} must be greater than V_T for the MOSFET to be in the saturation region, we select the solution

$$i_D = 0.5 \text{ mA} \qquad v_{GS} = 2 \text{ V}$$

The corresponding drain voltage is therefore found to be

$$v_D = v_{DD} - R_D i_D = 10 - 6i_D = 7 \text{ V}$$

And therefore

$$v_{DS} = v_D - v_S = v_D - i_D R_S = 7 - 3 = 4 \text{ V}$$

Comments: Now that we have computed the desired voltages and current, we can verify that the conditions for operation in the saturation region are indeed satisfied: $v_{GS} = 2 > V_T$ and $v_{GD} = v_{GS} - v_{DS} = 2 - 4 = -2 < V_T$. Since the inequalities are satisfied, the MOSFET is indeed operating in the saturation region.

Operation of the *P*-Channel Enhancement-Mode MOSFET

The operation of a p-channel enhancement-mode MOS transistor is very similar in concept to that of an n-channel device. Figure 11.10 depicts a test circuit and a sketch of the device construction. Note that the roles of n-type and p-type materials are reversed and that the charge carriers in the channel are no longer electrons, but holes. Further, the threshold voltage is now negative: $V_T < 0$. However, if we replace v_{GS} with v_{SG}, v_{GD} with v_{DG}, and v_{DS} with v_{SD}, and we use $|V_T|$ in place of V_T, then the

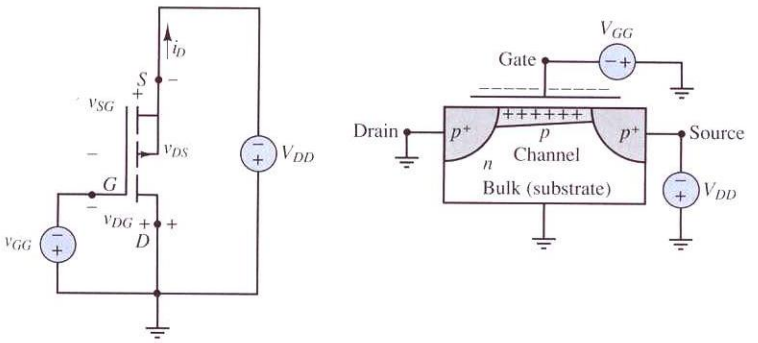

Figure 11.10 The p-channel enhancement-mode field-effect transistor (PMOS)

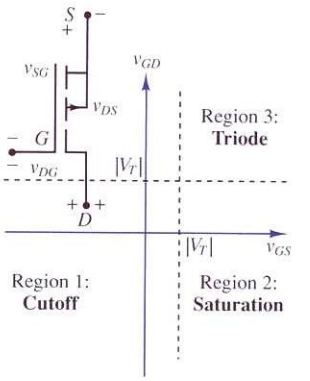

Figure 11.11 Regions of operation of PMOS transistor

analysis of the device is completely analogous to that of the n-channel MOS transistor. In particular, Figure 11.11 depicts the behavior of a PMOS transistor in terms of the gate-to-drain and gate-to-source voltages, in analogy with Figure 11.4. The resulting equations for the three modes of operation of the PMOS transistor are summarized below:

Cutoff region: $v_{SG} < |V_T|$ and $v_{DG} < |V_T|$.

$$i_D = 0 \qquad \text{Cutoff region} \tag{11.5}$$

Saturation region: when $v_{SG} > |V_T|$ and $v_{DG} < |V_T|$.

$$i_D \cong K(v_{SG} - |V_T|)^2 \qquad \text{Saturation region} \tag{11.6}$$

Triode or ohmic region: when $v_{SG} > |V_T|$ and $v_{DG} > |V_T|$.

$$i_D = K[2(v_{SG} - |V_T|)v_{SD} - v_{SD}^2] \qquad \text{Triode or ohmic region} \tag{11.7}$$

11.4 MOSFET LARGE-SIGNAL AMPLIFIERS

The objective of this section is to illustrate how a MOSFET can be used as a large signal amplifier, in applications similar to those illustrated in Chapter 10 for bipolar transistors. Equation 11.3, repeated below for convenience, describes the approximate relationship between the drain current and gate-source voltage for the MOSFET in a large-signal amplifier application. Appropriate biasing, as explained in the preceding section, is used to ensure that the MOSFET is operating in the saturation mode.

$$i_D \cong K(v_{GS} - V_T)^2 \tag{11.8}$$

MOSFET amplifiers are commonly found in one of two configurations: *common-source* and *source-follower* amplifiers. Figure 11.12 depicts a basic common-source configuration. Note that when the MOSFET is in saturation, this amplifier is essentially a voltage-controlled current source (VCCS), in which the drain current is

11.5 MOSFET SWITCHES

The objective of this section is to illustrate how a MOSFET can be used as an analog or a digital switch (or gate). Most MOSFET switches make use of a particular technology known as **complementary metal-oxide semiconductor,** or **CMOS.** CMOS technology makes use of the complementary characteristics of PMOS and NMOS devices and leads to the design of integrated circuits with extremely low power consumption. Further, CMOS circuits are easily fabricated and require a single supply voltage, which is a significant advantage.

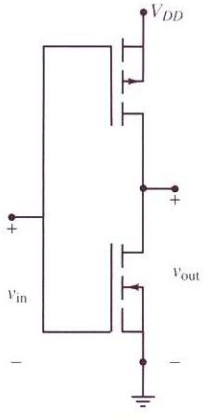

Figure 11.16 CMOS inverter

Digital Switches and Gates

To explain CMOS technology, we make reference to the **CMOS inverter** of Figure 11.16, in which two p-channel and n-channel enhancement-mode devices are connected so as to have a single supply voltage (V_{DD}, relative to ground) and so that their gates are tied together. The p-channel transistor is shown on the top and the n-channel device on the bottom in Figure 11.16. Functionally, this device is an inverter in the sense that whenever the input voltage v_{in} is *logic high*, or 1 (i.e., near V_{DD}), then the output voltage is *logic low* (or 0). If the input is logic 0, on the other hand, then the output will be logic 1.

The operation of the inverter is as follows. When the input voltage is high (near V_{DD}), then the gate-to-source voltage for the p-channel transistor is near zero and the PMOS transistor operates in the cutoff region. Thus, no drain current flows through the top transistor, and it is *off*, acting as an open circuit. On the other hand, with v_{in} near V_{DD}, the bottom transistor sees a large gate-to-source voltage and will turn *on*, resulting in a small resistance between the v_{out} terminal and ground. Thus, if v_{in} is "high," v_{out} will by necessity be "low." This is illustrated in the simplified sketch of Figure 11.17(a), in which the PMOS transistor is approximated by an open switch (to signify the off condition) and the NMOS transistor is shown as a closed switch to denote its on condition. When the input voltage is low (near 0 V), then the PMOS transistor will see a large negative gate-to-source voltage and will turn on; on the other hand, the gate-to-source voltage for the NMOS will be near zero, and the lower transistor will be off. This is illustrated in Figure 11.17(b), using ideal

LO5

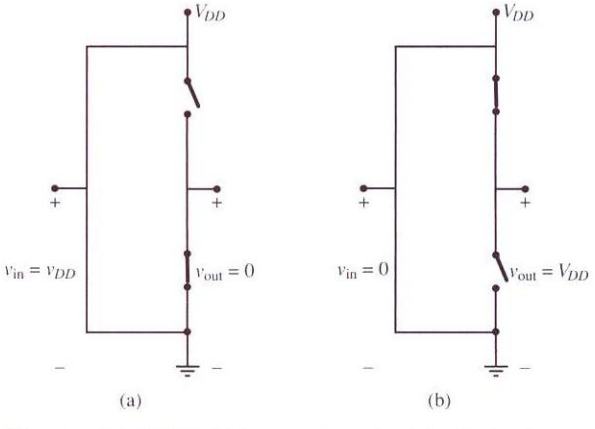

Figure 11.17 CMOS inverter approximate by ideal switches: (a) When v_{in} is "high," v_{out} is tied to ground; (b) when v_{in} is "low," v_{out} is tied to V_{DD}.

switches to approximate the individual transistors. Note that this simple logic inverter does not require the use of any resistors to bias the transistors: it is completely self-contained and very easy to fabricate. Further, it is also characterized by very low power consumption, making it ideal for many portable consumer electronic applications.

Examples 11.8 and 11.9 illustrate a number of digital switch and gate applications of MOS technology. Example 11.8 explores a NMOS switch using the drain characteristic curves; Example 11.9 analyzes a digital logic gate built using CMOS technology.

EXAMPLE 11.8 MOSFET Switch

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Problem

Determine the operating points of the MOSFET switch of Figure 11.18 when the signal source output is equal to 0 and 2.5 V, respectively.

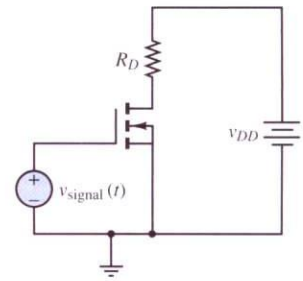


Figure 11.18

Solution

Known Quantities: Drain resistor; V_{DD}; signal source output voltage as a function of time.

Find: Q point for each value of the signal source output voltage.

Schematics, Diagrams, Circuits, and Given Data: $R_D = 125\ \Omega$; $V_{DD} = 10$ V; $v_{signal}(t) = 0$ V for $t < 0$; $v_{signal}(t) = 2.5$ V for $t = 0$.

Assumptions: Use the drain characteristic curves for the MOSFET (Figure 11.19).

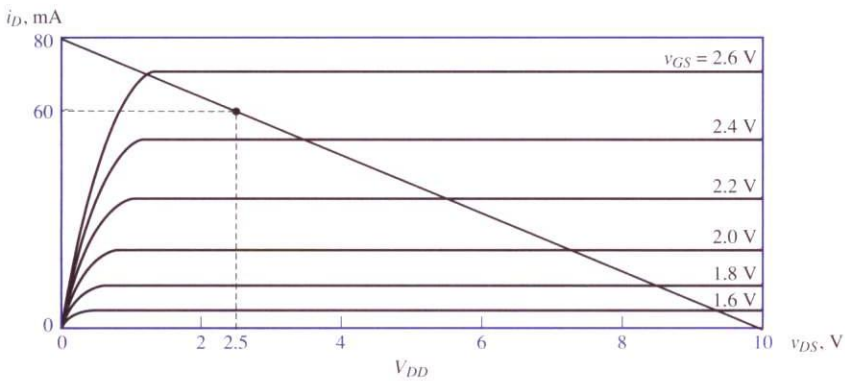


Figure 11.19 Drain curves for MOSFET of Figure 11.18

Analysis: We first draw the load line, using the drain circuit equation

$$V_{DD} = R_D i_D + v_{DS} \qquad 10 = 125 i_D + v_{DS}$$

recognizing a v_{DS} axis intercept at 10 V and an i_D axis intercept at $10/125 = 80$ mA.

1. $t < 0$ s. When the signal source output is zero, the gate voltage is zero and the MOSFET is in the cutoff region. The Q point is

$$v_{GSQ} = 0\ \text{V} \qquad i_{DQ} = 0\ \text{mA} \qquad v_{DSQ} = 10\ \text{V}$$

2. $t \geq 0$ s. When the signal source output is 2.5 V, the gate voltage is 2.5 V and the MOSFET is in the saturation region. The Q point is

$$v_{GSQ} = 0 \text{ V} \qquad i_{DQ} = 60 \text{ mA} \qquad v_{DSQ} = 2.5 \text{ V}$$

This result satisfies the drain equation, since $R_D i_D = 0.06 \times 125 = 7.5$ V.

Comments: The simple MOSFET configuration shown can quite effectively serve as a switch, conducting 60 mA when the gate voltage is switched to 2.5 V.

CHECK YOUR UNDERSTANDING

What value of R_D would ensure a drain-to-source voltage v_{DS} of 5 V in the circuit of Example 11.8?

Answer: 62.5 Ω

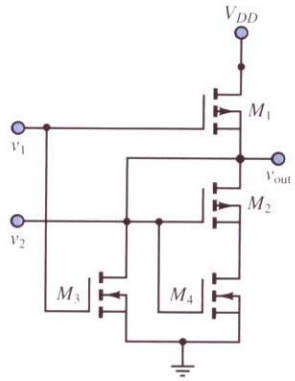
LO5

EXAMPLE 11.9 CMOS Gate

Problem

Determine the logic function implemented by the CMOS gate of Figure 11.20. Use the table below to summarize the behavior of the circuit.

v_1	v_2	State of M_1	State of M_2	State of M_3	State of M_4	v_{out}
0 V	0 V					
0 V	5 V					
5 V	0 V					
5 V	5 V					



The transistors in this circuit show the substrate for each transistor connected to its respective gate. In a true CMOS IC, the substrates for the p-channel transistors are connected to 5 V and the substrates of the n-channel transistors are connected to ground.

Figure 11.20

Solution

Find: v_{out} for each of the four combinations of v_1 and v_2.

Schematics, Diagrams, Circuits, and Given Data: $V_T = 1.7$ V; $V_{DD} = 5$ V.

Assumptions: Treat the MOSFETs as open circuits when off and as linear resistors when on.

Analysis:

1. $v_1 = v_2 = 0$ V. With both input voltages equal to zero, neither M_3 nor M_4 can conduct, since the gate voltage is less than the threshold voltage for both transistors. Both M_1 and M_2 will similarly be off, and no current will flow through the drain-source circuits of M_1 and M_2. Thus, $v_{out} = V_{DD} = 5$ V. This condition is depicted in Figure 11.21.
2. $v_1 = 5$ V; $v_2 = 0$ V. Now M_2 and M_4 are off because of the zero gate voltage, while M_1 and M_3 are on. Figure 11.22(a) depicts this condition. Thus, $v_{out} = 0$.
3. $v_1 = 5$ V; $v_2 = 0$ V. By symmetry with case 2, we conclude that $v_{out} = 0$.
4. $v_1 = 5$ V; $v_2 = 5$ V. Now both M_1 and M_2 are open circuits, and therefore $v_{out} = 0$.

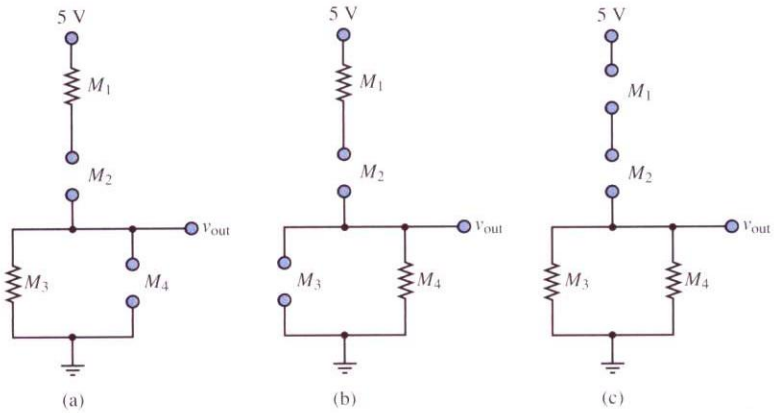
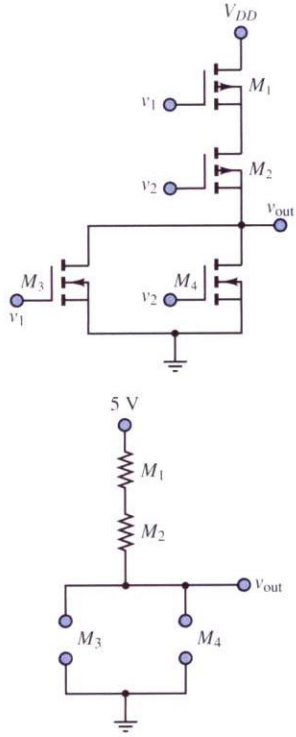


Figure 11.22



With both v_1 and v_2 at 0 V, M_3 and M_4 will be turned off (in cutoff), since v_{GS} is less than V_T (0 V < 1.7 V). Both M_1 and M_2 will be turned on, since the gate-to-source voltages will be greater than V_T.

Figure 11.21

These results are summarized in the table below. The output voltage for case 4 is sufficiently close to zero to be considered zero for logic purposes.

v_1	v_2	M_1	M_2	M_3	M_4	v_{out}
0 V	0 V	On	On	Off	Off	5 V
0 V	5 V	On	Off	Off	Off	0 V
5 V	0 V	Off	On	Off	On	0 V
5 V	5 V	Off	Off	On	On	0 V

Thus, the gate is a NOR gate.

Comments: While exact analysis of CMOS gate circuits could be tedious and involved, the method demonstrated in this example—to determine whether transistors are on or off—leads to very simple analysis. Since in logic devices one is interested primarily in logic levels and not in exact values, this approximate analysis method is very appropriate.

CHECK YOUR UNDERSTANDING

Analyze the CMOS gate of Figure 11.23 and find the output voltages for the following conditions: (a) $v_1 = 0$, $v_2 = 0$; (b) $v_1 = 5$ V, $v_2 = 0$; (c) $v_1 = 0$, $v_2 = 5$ V; (d) $v_1 = 5$ V, $v_2 = 5$ V. Identify the logic function accomplished by the circuit.

Answer:

NAND gate

v_1	v_2	v_{out}
0 V	5 V	5 V
5 V	5 V	0 V
5 V	0 V	5 V
5 V	0 V	0 V
0 V	5 V	5 V

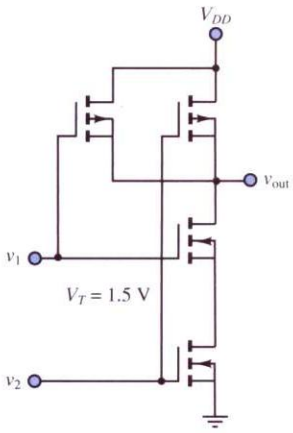


Figure 11.23 CMOS gate

Analog Switches

A common form of analog gate employs a FET and takes advantage of the fact that current can flow in either direction in a FET biased in the ohmic region. Recall that the drain characteristic of the MOSFET discussed in Section 11.2 consists of three regions: ohmic, active, and breakdown. A MOSFET amplifier is operated in the active region, where the drain current is nearly constant for any given value of v_{GS}. On the other hand, a MOSFET biased in the ohmic state acts very much as a linear resistor. For example, for an n-channel enhancement MOSFET, the conditions for the transistor to be in the ohmic region are

$$v_{GS} > V_T \qquad \text{and} \qquad |v_{DS}| \leq \frac{1}{4}(v_{GS} - V_T) \tag{11.13}$$

As long as the FET is biased within these conditions, it acts simply as a linear resistor, and it can conduct current in either direction (provided that v_{DS} does not exceed the limits stated in equation 11.13). In particular, the resistance of the channel in the ohmic region is found to be

$$r_{DS} = \frac{1}{2K(v_{GS} - V_T)} \tag{11.14}$$

so that the drain current is equal to

$$i_D \approx \frac{v_{DS}}{r_{DS}} \qquad \text{for} \quad |v_{DS}| \leq \frac{1}{4}(v_{GS} - V_T) \quad \text{and} \quad v_{GS} > V_T \tag{11.15}$$

The most important feature of the MOSFET operating in the ohmic region, then, is that it acts as a voltage-controlled resistor, with the gate-source voltage v_{GS} controlling the channel resistance R_{DS}. The use of the MOSFET as a switch in the ohmic region, then, consists of providing a gate-source voltage that can either hold the MOSFET in the cutoff region ($v_{GS} \leq V_T$) or bring it into the ohmic region. In this fashion, v_{GS} acts as a control voltage for the transistor.

Consider the circuit shown in Figure 11.24, where we presume that v_C can be varied externally and that v_{in} is some analog signal source that we may wish to connect to the load R_L at some appropriate time. The operation of the switch is as follows. When $v_C \leq V_T$, the FET is in the cutoff region and acts as an open circuit.

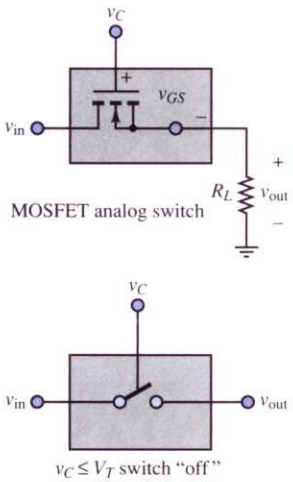
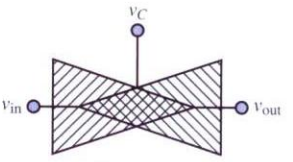


Figure 11.24 MOSFET analog switch

When $v_C > V_T$ (with a value of v_{GS} such that the MOSFET is in the ohmic region), the transistor acts as a linear resistance R_{DS}. If $R_{DS} \ll R_L$, then $v_{out} \approx v_{in}$. By using a pair of MOSFETs, it is possible to improve the dynamic range of signals one can transmit through this analog gate.

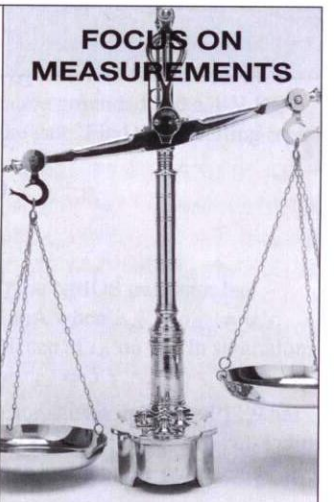
MOSFET analog switches are usually produced in integrated-circuit (IC) form and denoted by the symbol shown in Figure 11.25. A CMOS analog gate is described in the next Focus on Measurements box.



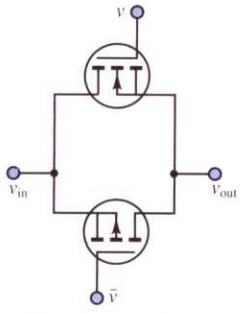
$v_C = V \Rightarrow$ on state
$v_C = -V \Rightarrow$ off state

Figure 11.25 Symbol for bilateral FET analog gate

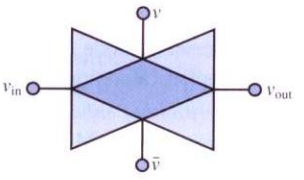
MOSFET Bidirectional Analog Gate



The variable-resistor feature of MOSFETs in the ohmic state finds application in the **analog transmission gate.** The circuit shown in Figure 11.26 depicts a circuit constructed using CMOS technology. The circuit operates on the basis of a control voltage v that can be either "low" (say, 0 V) or "high" ($v > V_T$), where V_T is the threshold voltage for the n-channel MOSFET and $-V_T$ is the threshold voltage for the p-channel MOSFET. The circuit operates in one of two modes. When the gate of Q_1 is connected to the high voltage and the gate of Q_2 is connected to the low voltage, the path between v_{in} and v_{out} is a relatively small resistance, and the transmission gate conducts. When the gate of Q_1 is connected to the low voltage and the gate of Q_2 is connected to the high voltage, the transmission gate acts as a very large resistance and is an open circuit for all practical purposes. A more precise analysis follows.



(a) CMOS transmission gate



(b) CMOS transmission gate circuit symbol

Figure 11.26 Analog transmission gate

Let $v = V > V_T$ and $\bar{v} = 0$. Assume that the input voltage v_{in} is in the range $0 \le v_{in} \le V$. To determine the state of the transmission gate, we consider only the extreme cases $v_{in} = 0$ and $v_{in} = V$. When $v_{in} = 0$, $v_{GS1} = v - v_{in} = V - 0 = V > V_T$. Since V is above the threshold voltage, MOSFET Q_1 conducts (in the ohmic region). Further, $v_{GS2} = \bar{v} - v_{in} = 0 > -V_T$. Since the gate-source voltage is not more negative than the threshold voltage, Q_2 is in cutoff and does not conduct. Since one of the two possible paths between v_{in} and v_{out} is conducting, the transmission gate is on. Now consider the other extreme, where $v_{in} = V$. By reversing the previous argument, we can see that Q_1 is now off, since $v_{GS1} = 0 < V_T$. However, now Q_2 is in the ohmic state, because $v_{GS2} = \bar{v} - v_{in} = 0 - V < -V_T$. In this case, then, it is Q_2

(*Continued*)

(*Concluded*)

that provides a conducting path between the input and the output of the transmission gate, and the transmission gate is also on. We have therefore concluded that when $v = V$ and $\overline{v} = 0$, the transmission gate conducts and provides a near-zero-resistance (typically tens of ohms) connection between the input and the output of the transmission gate, for values of the input ranging from 0 to V.

Let us now reverse the control voltages and set $v = 0$ and $\overline{v} = V > V_T$. It is very straightforward to show that in this case, regardless of the value of v_{in}, both Q_1 and Q_2 are always off; therefore, the transmission gate is essentially an open circuit.

The analog transmission gate finds common application in *analog multiplexers* and *sample-and-hold* circuits, to be discussed in Chapter 15.

CHECK YOUR UNDERSTANDING

Show that the CMOS bidirectional gate described in the Focus on Measurements box "MOSFET Bidirectional Analog Gate" is off for all values of v_{in} between 0 and V whenever $v = 0$ and $\overline{v} = V > V_T$.

Conclusion

This chapter has introduced field-effect transistors, focusing primarily on metal-oxide semiconductor enhancement-mode n-channel devices to explain the operation of FETs as amplifiers. A brief introduction to p-channel devices is used as the basis to introduce CMOS technology, and to present analog and digital switches and logic gate applications of MOSFETs. Upon completing this chapter, you should have mastered the following learning objectives:

1. *Understand the classification of field-effect transistors.* FETs include three major families; the enhancement-mode family is the most commonly used and is the one explored in this chapter. Depletion-mode and junction FETs are only mentioned briefly.
2. *Learn the basic operation of enhancement-mode MOSFETs by understanding their i–v curves and defining equations.* MOSFETs can be described by the i–v drain characteristic curves, and by a set of nonlinear equations linking the drain current to the gate-to-source and drain-to-source voltages. MOSFETs can operate in one of four regions: *cutoff*, in which the transistor does not conduct current; *triode*, in which the transistor can act as a voltage-controlled resistor under certain conditions; *saturation*, in which the transistor acts as a voltage-controlled current source and can be used as an amplifier; and *breakdown* when the limits of operation are exceeded.
3. *Learn how enhancement-mode MOSFET circuits are biased.* MOSFET circuits can be biased to operate around a certain operating point, known as the Q point, by appropriately selecting supply voltages and resistors.
4. *Understand the concept and operation of FET large-signal amplifiers.* Once a MOSFET circuit is properly biased in the saturation region, it can serve as an amplifier by virtue of its voltage-controlled current source property: small changes in the gate-to-source voltages are translated to proportional changes in drain current.
5. *Understand the concept and operation of FET switches.* MOSFETs can serve as analog and digital switches: by controlling the gate voltage, a MOSFET can be turned on and off (digital switch), or its resistance can be modulated (analog switch).
6. *Analyze FET switches and digital gates.* These devices find application in CMOS circuits as digital logic gates and analog transmission gates.